REMARKS

Claims 1, 3-4 and 11-24 are pending in the application, as amended. Applicant amends paragraphs [para 7] and [para 11] to correct typographical errors in the originally filed application. No new matter was entered by the amendment to the Specification. The amendments are supported by the originally filed Specification. Applicant amends claims 1 and 3-4 and has added new claims 11-24 to better describe the invention as disclosed in the original application. Claims 2 and 5-10 have been cancelled. The amendments are supported by the originally filed claims and in the original Specification at paragraphs [Para 22]-[Para 29], among other places. Accordingly, no new matter was entered.

Prior Art Rejections

The Examiner rejected claims 1-10 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,829,682 to *Kirihata et al.* In light of the amendments identified above and the reasons below, Applicant respectfully requests withdrawal of all pending rejections.

Claim 1 as amended recites, among others:

> providing the bit line and the bit line bar with an initial bias, wherein the bit line has a first-status bias when the bit line is coupled to the charge storage device in the first status and the bit line has a second-status bias when the bit line is coupled to the charge storage device in the second status;
>
> providing the bit line bar with a sensing bias approximately when the bit line is coupled to the charge storage device, wherein the sensing bias is different from the initial bias of the bit line and is between the first-status bias and the second-status bias...

Similarly, newly added claim 17 recites, among others:

> providing the bit line and the bit line bar with an initial bias, wherein the bit line has a first-status bias when the bit line is coupled to the charge storage device in the first status and the bit line has a second-status bias when the bit line is coupled to the charge storage device in the second status;
>
> providing the bit line bar with a sensing bias approximately when the bit line is coupled to the charge storage device, wherein the sensing bias is between the first-status bias and the second-status bias...

In contrast, *Kirihata et al.* relates to a destructive read architecture for dynamic random access memories. *Kirihata et al.* disclose a method for controlling a DRAM by enabling a destructive read mode and a delayed write back mode. (Col. 1, lines 40-55). *Kirihata et al.* fail to teach or suggest providing the bit line and the bit line bar with an initial bias of a certain level. Specifically, nowhere does *Kirihata et al.* teach or suggest "providing the bit line and the bit line bar with an initial bias, wherein the bit line has a first-status bias when the bit line is coupled to the charge storage device in the first status and the bit line has a second-status bias when the bit line is coupled to the charge storage device in the second status" and "providing the bit line bar with a sensing bias approximately when the bit line is coupled to the charge storage device, wherein the sensing bias . . . is between the first-status bias and the second-status bias…", as recited in claims 1 and 17.

For at least these reasons, independent claims 1 and 17 are patentable over *Kirihata et al.* Additionally, claims 3-4 and 11-16 and 18-24, which depend from claims 1 and 17, respectively, are also patentable at least because they depend from allowable base claims and because they each recite additional patentable features and/or elements.

CONCLUSION

For at least the reasons above, Applicant respectfully submits that the instant application, including claims 1, 3-4 and 11-24, is in condition for allowance.

Respectfully submitted,

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